UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/068,251 | 02/06/2002 | Eric Yean-Liu Chang | JCLA7357 | 8504 |

7590 07/08/2004

J.C. Patents, Inc.
Suite 250
4 Venture
Irvine, CA 92618

| EXAMINER | |
|---|---|
| TORRES, JOSEPH D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | 3 |

DATE MAILED: 07/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 10/068,251 | Applicant(s) CHANG ET AL. | |
|---|---|---|---|
| | Examiner Joseph D. Torres | Art Unit 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 May 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-8* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-5, drawn to A Memory Control Device for Controlling a Memory Unit comprising: a Command Decoding Device; a Compare Logic Device Coupled to the Command Decoding Device; a Frame Buffer Decode Device; a Decision Device Coupled to the Command Decoding Device, the Compare Logic Device and the Frame Buffer Decode Device; and a Command Routing Device Coupled to the Decision Device; classified in class 714, subclass 763.

II. Claims 6 and 7, drawn to A Memory Control Method comprising a Step for Checking if the Access Address Points to a Memory Bank Range having an Error-Check-Correction Function but Outside a Graphic Memory Range, classified in class 714, subclass 702.

III. Claim 8, drawn to A Memory Control Method comprising a Step for Disabling an Error-Check-Correction Function if the Access Address Points to a Memory Bank Range having an Error-Check-Correction Function and Inside a Frame Buffer Range, classified in class 714, subclass 708.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group II, A Memory Control Method comprising a Step for Checking if the Access Address Points to a Memory Bank Range having an Error-Check-Correction Function but Outside a Graphic Memory Range, and Group I, A Memory Control Device for Controlling a Memory Unit comprising: a Command Decoding Device; a Compare Logic Device Coupled to the Command Decoding Device; a Frame Buffer Decode Device; a Decision Device Coupled to the Command Decoding Device, the Compare Logic Device and the Frame Buffer Decode Device; and a Command Routing Device Coupled to the Decision Device, are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process Group II, A Memory Control Method comprising a Step for Checking if the Access Address Points to a Memory Bank Range having an Error-Check-Correction Function but Outside a Graphic Memory Range, as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus Group I, A Memory Control Device for Controlling a Memory Unit comprising: a Command Decoding Device; a Compare Logic Device Coupled to the Command Decoding Device; a Frame Buffer Decode Device; a Decision Device Coupled to the Command Decoding Device, the Compare Logic Device and the Frame Buffer Decode Device; and a Command Routing Device Coupled to the Decision Device, as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the process can be use for checking if the access address points to a memory bank range having an error-check-correction function but outside a graphic memory range and the apparatus does not require such a step.

Inventions Group III, A Memory Control Method comprising a Step for Disabling an Error-Check-Correction Function if the Access Address Points to a Memory Bank Range having an Error-Check-Correction Function and Inside a Frame Buffer Range, and Group I, A Memory Control Device for Controlling a Memory Unit comprising: a Command Decoding Device; a Compare Logic Device Coupled to the Command Decoding Device; a Frame Buffer Decode Device; a Decision Device Coupled to the Command Decoding Device, the Compare Logic Device and the Frame Buffer Decode Device; and a Command Routing Device Coupled to the Decision Device, are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process Group III, A Memory Control Method comprising a Step for Disabling an Error-Check-Correction Function if the Access Address Points to a Memory Bank Range having an Error-Check-Correction Function and Inside a Frame Buffer Range, as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus Group I, A Memory Control Device for Controlling a Memory Unit comprising: a Command Decoding Device; a Compare Logic Device Coupled to the Command Decoding Device; a Frame Buffer Decode Device; a Decision Device Coupled to the Command Decoding Device, the Compare Logic Device and the Frame Buffer Decode Device; and a Command Routing Device Coupled to the Decision Device, as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the process can be use for disabling an error-check-correction function if the access address points to a memory bank range having an

error-check-correction function and inside a frame buffer range and the apparatus does not require such a step.

Inventions Group II, A Memory Control Method comprising a Step for Checking if the Access Address Points to a Memory Bank Range having an Error-Check-Correction Function but Outside a Graphic Memory Range, and Group III, A Memory Control Method comprising a Step for Disabling an Error-Check-Correction Function if the Access Address Points to a Memory Bank Range having an Error-Check-Correction Function and Inside a Frame Buffer Range, are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group II, A Memory Control Method comprising a Step for Checking if the Access Address Points to a Memory Bank Range having an Error-Check-Correction Function but Outside a Graphic Memory Range, has separate utility such as for checking if the access address points to a memory bank range having an error-check-correction function but outside a graphic memory range. In the instant case, invention Group III, A Memory Control Method comprising a Step for Disabling an Error-Check-Correction Function if the Access Address Points to a Memory Bank Range having an Error-Check-Correction Function and Inside a Frame Buffer Range, has separate utility such as for disabling an error-check-correction function if the access address points to a memory bank range having an error-check-correction function and inside a frame buffer range. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group III and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group III and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

A telephone call was made to Jiawei Huang on 30 June 2004 to request an oral election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133